FIG. 1

. . .

Target Address	Operands & Working Registers	PC	Code
	Additional Data Payload		
	PARCEL FORMAT		
HEAVYWEIGHT ISA PROCESSING  CACHE  PIGLET PROCESSING  "CLASSICAL" HOST CPU NODE	PARCEL NETWORK INTERCONNECT		IOCAL IOCAL IOCAL ISA PROCESSING  MEMORY  LOCAL ADDRESS MANAGEMENT  PIGLET PROCESSING

FIG. 2

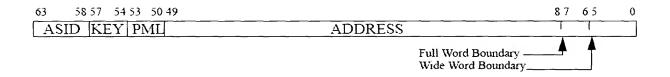


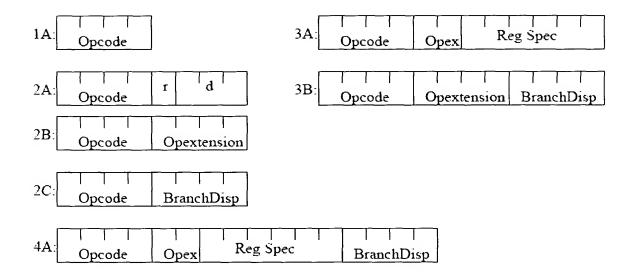
FIG. 3

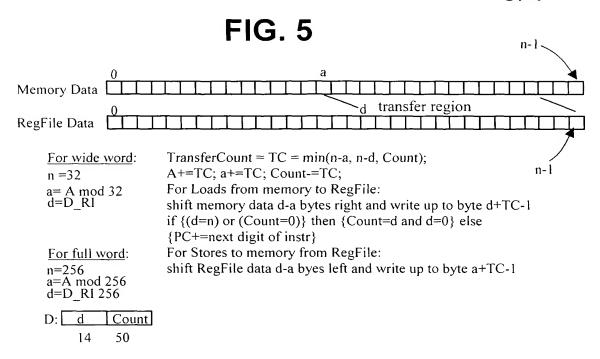
	A	D	R	F,S,PC C[4]C[15]		
W[0]	E[0]	E[1]	E[2]	E[3]		
W[1]	E[4]	E[5]	E[6]	E[7]		
W[2]	E[8]	E[9]	E[10]	E[11]		
W[3]	E[12]	<b>E[13]</b>	E[14] 6	* E[15] *		
W[4]	. E[16]	E[17].	E[18] 🚸	E[19]		
W[5]	E[20]	E[21]	E[22]	E[23]		
W[6]	E[24]	E[25]	E[26]	E[27]		
W[7]	E[28]	E[29]	E[30]	E[31]		
E[i] contains C[16+16i] through C[31+16i]  Present only in extended formats						

U is made up of W[0] through W[7]

Present only in 2304 bit formats

## FIG. 4





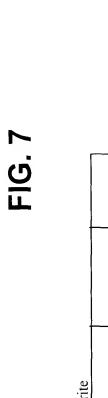
Wide Word DataOut

MEMORY Address THREADLET SHIFT W[0..7]
MACRO STATE MATRIX (U)

Write Mask

Wide Word DataIn

Parcel Interface



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